IN THE CLAIMS

Please amend the claims as follows:

1-17. (Canceled)

18. (New) A semiconductor device comprising:

a data memory which stores data;

a code memory which stores an ECC code for a test corresponding to the data;

an ECC circuit which supplies the data memory with a test pattern for detecting a bit error for all cells of the data memory, generates code data as the ECC code from the test pattern using a Hamming matrix which meets predetermined conditions, and supplies the code memory with the code data, the ECC circuit generating the code data for detecting a bit error for all cells of the code memory using a transposed matrix of the test pattern and the Hamming matrix; and

a test circuit which simultaneously tests the data memory and the code memory based on the test pattern written in the data memory and the code data generated by the ECC circuit.

19. (New) The semiconductor device according to claim 18, wherein the ECC circuit generates the code data using the Hamming matrix configured so that a sum of row components of the matrix is odd as the predetermined conditions.

20. (New) The semiconductor device according to claim 18, wherein the ECC circuit generates the code data using the Hamming matrix configured so that all bits of the code data change from "0" to "1" or from "1" to "0" in accordance with an inputting of the test pattern as the predetermined conditions.

21. (New) The semiconductor device according to claim 18, wherein the ECC circuit generates the code data using the Hamming matrix configured so that arbitrary N (N is a natural number equal to or greater than 2) bits of the same address cover all patterns of N-bit

combination in accordance with the inputting of the test pattern as the predetermined conditions.

22. (New) The semiconductor device according to claim 18, wherein the ECC circuit generates the code data using the Hamming matrix configured so that when all bits of the test pattern other than one specified bit are "1"s, all the bits of the code data generated from the test pattern are "1"s as the predetermined conditions.

23. (New) A method of memory test which is applied to a semiconductor device including a data memory which stores data and a code memory which stores an ECC code for a test corresponding to the data, the method comprising the steps of:

generating a test pattern required to execute a test for detecting a bit error for all cells of the data memory;

outputting the test pattern to the data memory;

generating code data as the ECC code for detecting a bit error for all cells of the code memory using a Hamming matrix which meets predetermined conditions and a transposed matrix of the test pattern and the Hamming matrix; and

simultaneously testing the data memory and the code memory based on the test pattern written in the data memory and the code data generated.

24. (New) The method according to claim 23, wherein the step of generating the code data includes generating the code data using the Hamming matrix configured so that a sum of row components of the matrix is odd as the predetermined conditions.

25. (New) The method according to claim 23, wherein the step of generating the code data includes generating the code data using the Hamming matrix configured so that all bits of the code data change from "0" to "1" or from "1" to "0" in accordance with an inputting of the test pattern as the predetermined conditions.

26. (New) The method according to claim 23, wherein the step of generating the code data includes generating the code data using the Hamming matrix configured so that arbitrary N (N is a natural number equal to or greater than 2) bits of the same address cover all patterns of N-bit combination in accordance with the inputting of the test pattern as the predetermined conditions.

27. (New) The method according to claim 23, wherein the step of generating the code data includes generating the code data using the Hamming matrix configured so that when all bits of the test pattern other than one specified bit are "1"s, all the bits of the code data generated from the test pattern are "1"s as the predetermined conditions.